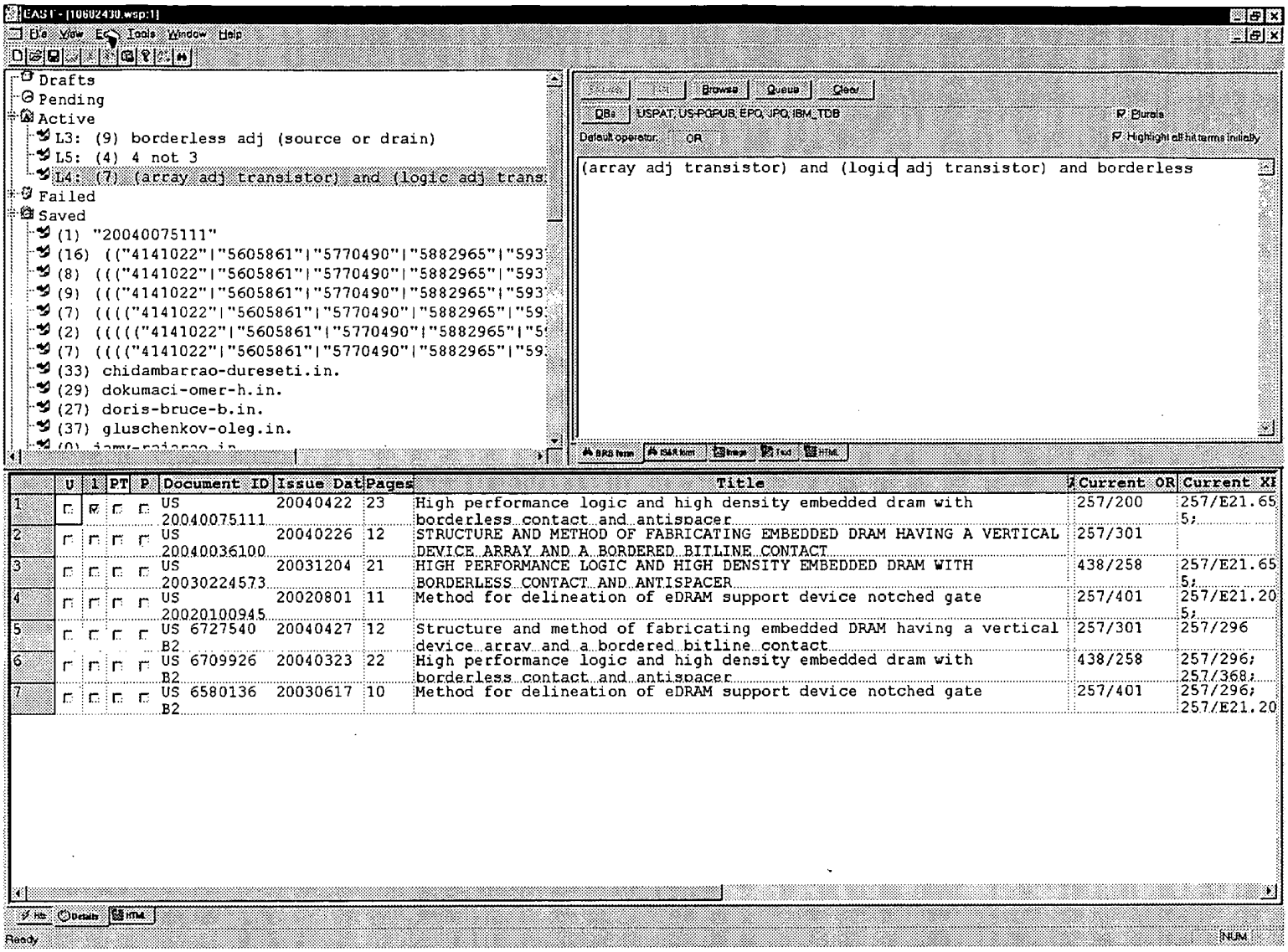

	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current XI
1	☐	☑	☐	☐	US 20040075111	20040422	23	High performance logic and high density embedded dram with borderless contact and antispacer	257/200	257/E21.655;
2	☐	☐	☐	☐	US 20040036100	20040226	12	STRUCTURE AND METHOD OF FABRICATING EMBEDDED DRAM HAVING A VERTICAL DEVICE ARRAY AND A BORDERED BITLINE CONTACT	257/301	
3	☐	☐	☐	☐	US 20030224573	20031204	21	HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER	438/258	257/E21.655;
4	☐	☐	☐	☐	US 20020100945	20020801	11	Method for delineation of eDRAM support device notched gate	257/401	257/E21.205;
5	☐	☐	☐	☐	US 6727540 B2	20040427	12	Structure and method of fabricating embedded DRAM having a vertical device array and a bordered bitline contact	257/301	257/296
6	☐	☐	☐	☐	US 6709926 B2	20040323	22	High performance logic and high density embedded dram with borderless contact and antispacer	438/258	257/296; 257/368;
7	☐	☐	☐	☐	US 6580136 B2	20030617	10	Method for delineation of eDRAM support device notched gate	257/401	257/296; 257/E21.20